

Multicore Computer Architecture - Storage and Interconnects

Lecture 18

Emerging Trends in Network On Chips



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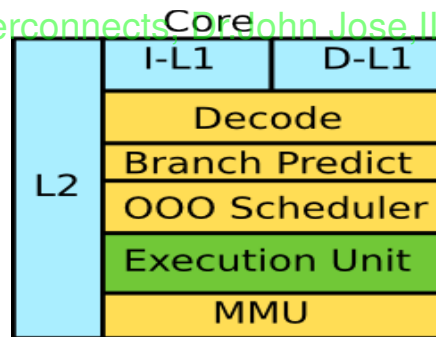
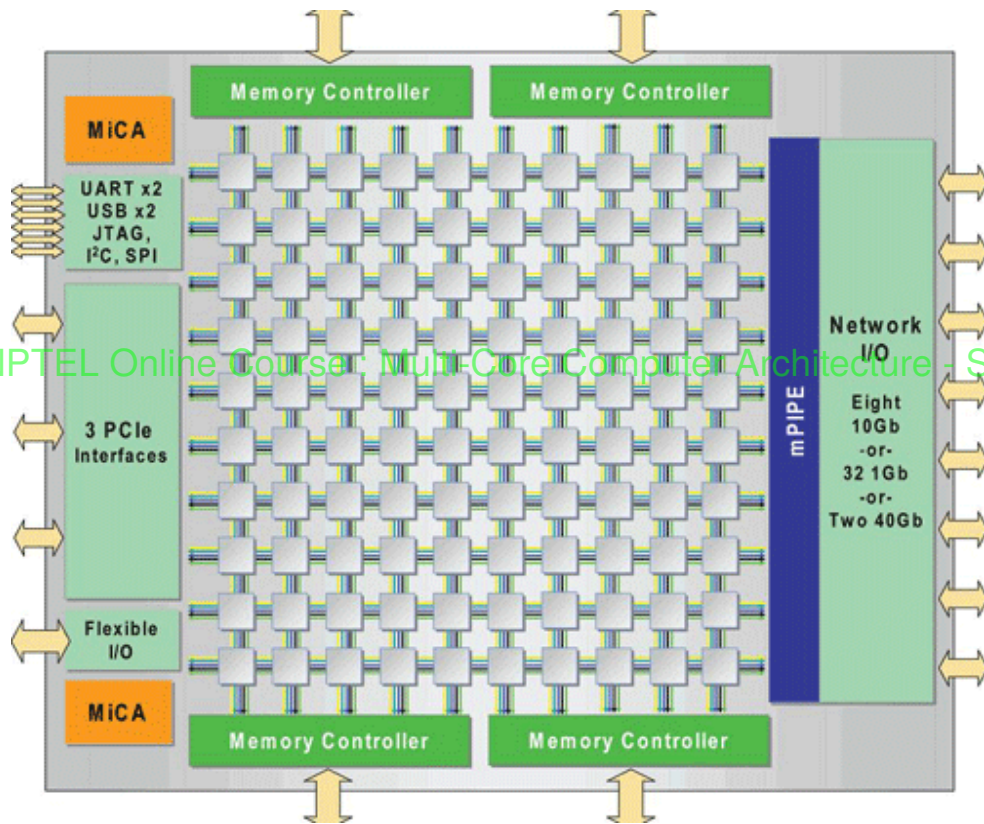
Dr. John Jose

Assistant Professor

Department of Computer Science & Engineering

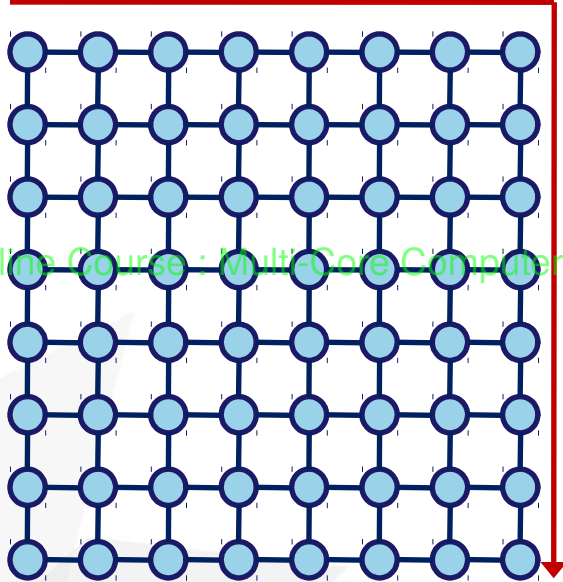
Indian Institute of Technology Guwahati, Assam.

Tiled Chip Multi Processors (TCMP)

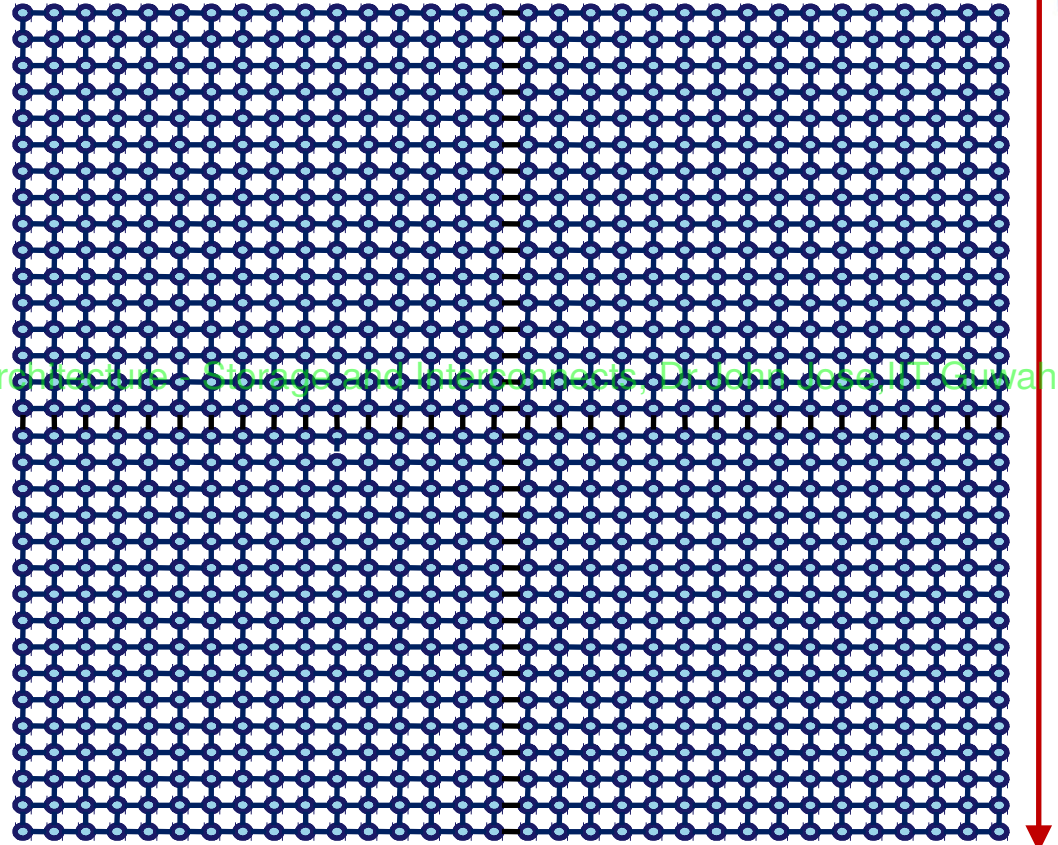


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Scaling of mesh architecture



8 X 8 2D mesh



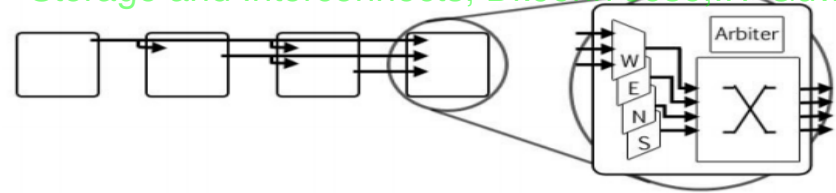
32 X 32 2D mesh

Emerging Trends in NoC

- ❖ Multidrop links
- ❖ Three-dimensional NoC
- ❖ RF interconnect
- ❖ Nanophotonic NoC
- ❖ Wireless NoC

Multi-drop Links

- ❖ Links where signals reach multiple routers in same clock cycle
- ❖ Reduces the diameter of the network without the need of very high radix routers
- ❖ These links are built up and broken down by sending bypass signals towards the destination



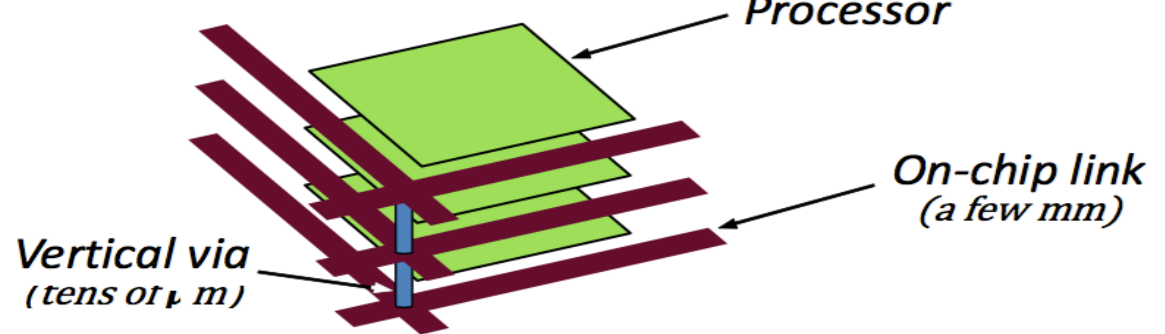
- B. Grot et al., "Kilo-NOC: A Heterogeneous Network-on-Chip Architecture for Scalability and Service Guarantees," ISCA-38, 2011
- T. Krishna, et al. "Single-Cycle Multihop Traversals over a Shared Network on Chip." IEEE Micro, 34(3), 2014

3D - NoC

❖ Benefits

- ❖ Higher packing density
- ❖ Improved noise immunity
- ❖ Overall superior performance

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- J. Burns *et al.*, "Three-dimensional integrated circuits for low-power, high-bandwidth systems on a chip," in IEEE ISSCC 2001

Vertical Interconnects

❖ Near-field coupling schemes

- Eliminate the need for a physical connection between layers
- Energy per transmission higher than state-of-the-art vias

❖ Inductive coupling schemes : Longer transmission ranges than capacitive ones for similar data rates

- N. Miura, *et al.* “A High-Speed Inductive-Coupling Link With Burst Transmission,” IEEE Journal of Solid-State Circuits, 44(3), 2009

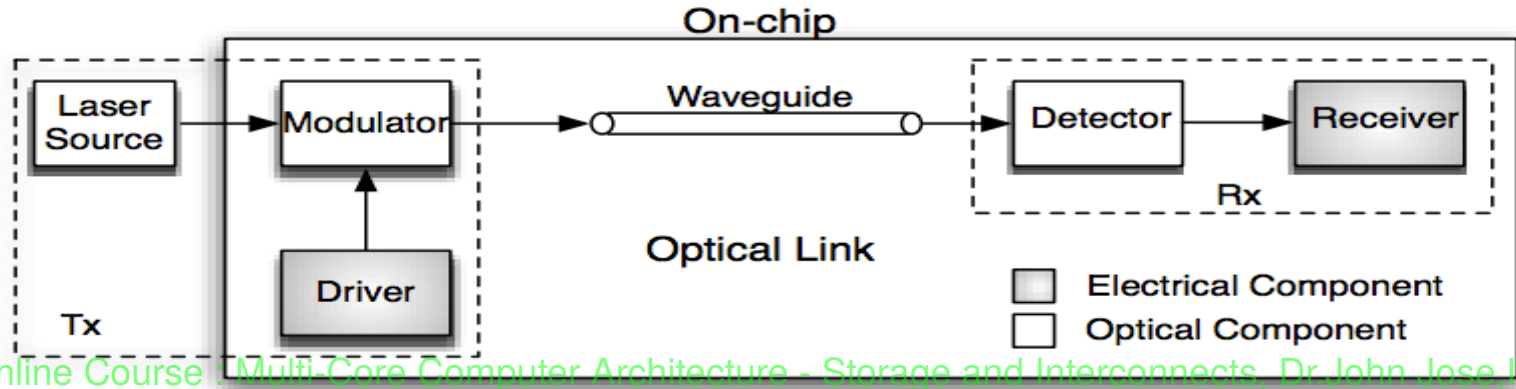
❖ Capacitive coupling schemes : Area overhead approximately one order of magnitude lower than the inductive options

- ❖ Q. Gu, *et al.* “Two 10Gb/s/pin Low-Power Interconnect Methods for 3D ICs,” Solid-State Circuits Conference, 2007

RF Interconnects

- ❖ Alternative to traditional VI signalling through metallic wires
- ❖ Transmission of electromagnetic waves over micro-strip transmission lines within the metal layers of the chip
- ❖ Signals are modulated using carrier waves at frequencies up to several GHz and then guided through the transmission lines
- ❖ Signals propagate at the speed of light instead of at the charging and discharging speed of RC wires, and need to be taken back at the baseband frequency and demodulated at the receiving end
 - M.-C. F. Chang, V. Roychowdhury, L. Zhang, H. Shin, and Y. Qian, “RF/wireless interconnect for inter and intra-chip communications,” Proceedings of the IEEE, vol. 89, no. 4, pp. 456–466, 2001

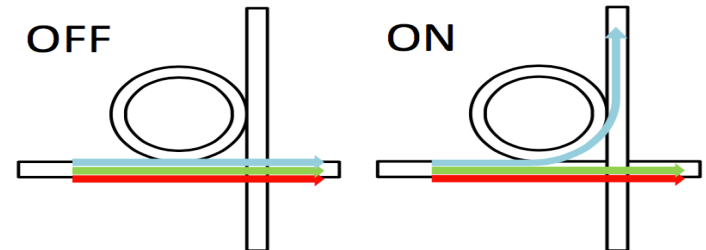
Nanophotonics



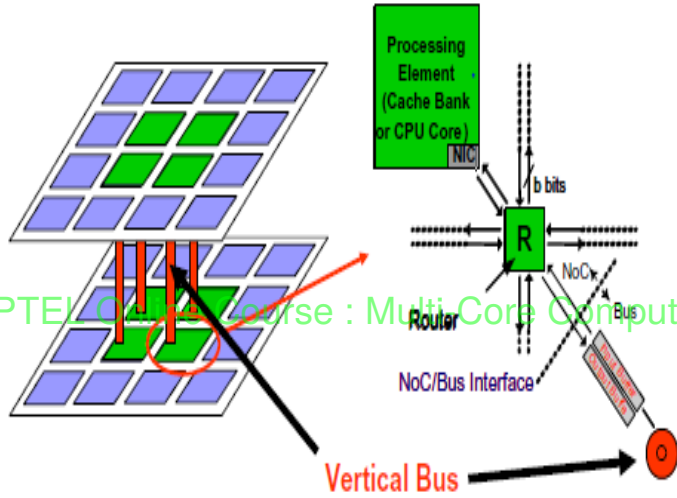
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❖ Microring resonators

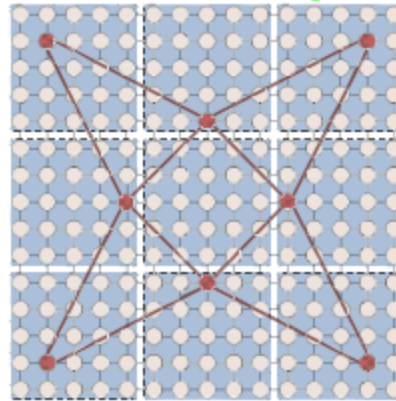
Divert light of a certain wavelength when a voltage is applied
Let light pass through otherwise



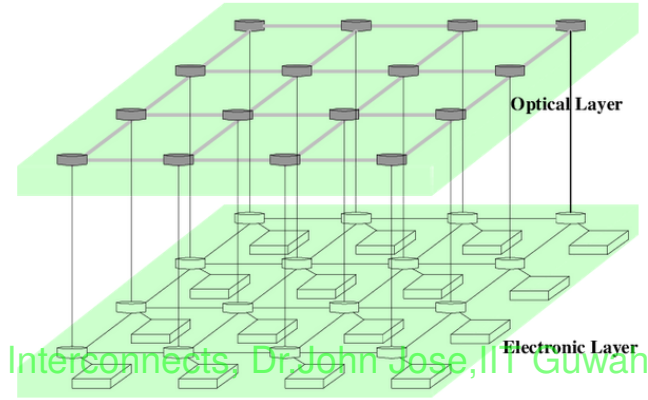
Emerging NoC Architectures



3D -NoC

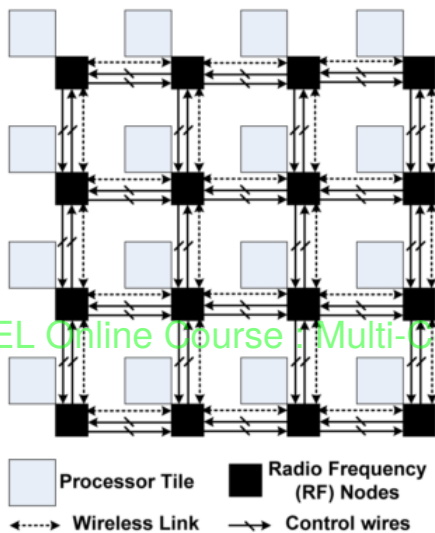


Wireless -NoC

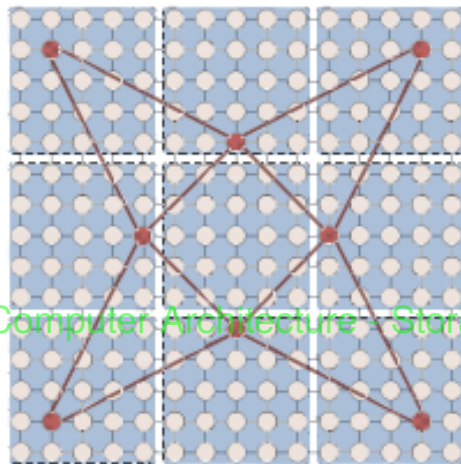


Photonic -NoC

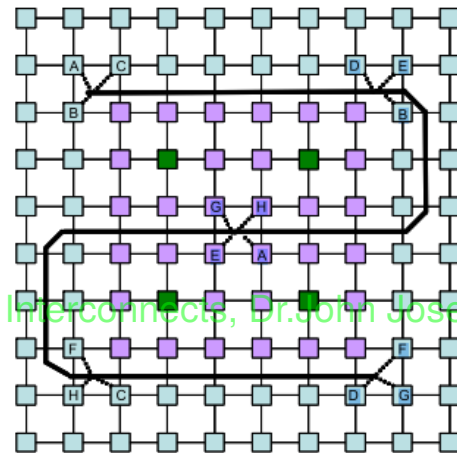
Different Wireless Architecture



UWB wireless connection

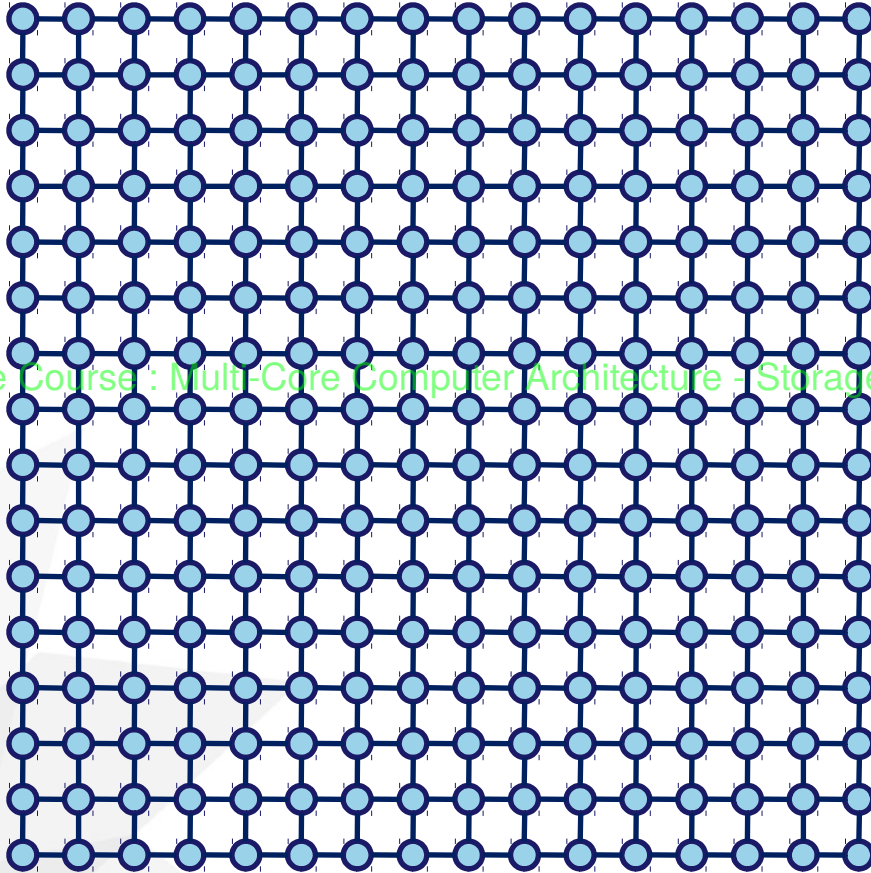


mm wave wireless connection



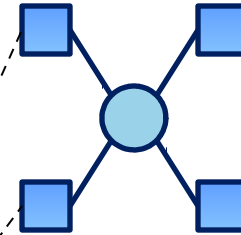
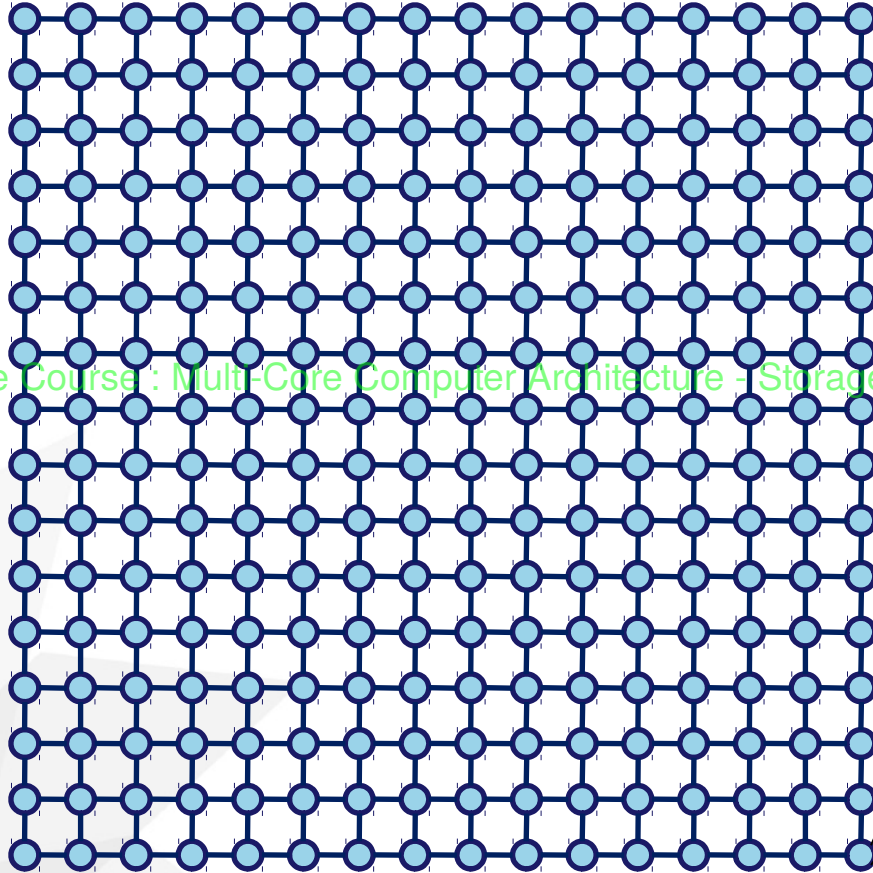
RF- waveguide wireless connection

16 X 16 Cmesh - 1024 cores

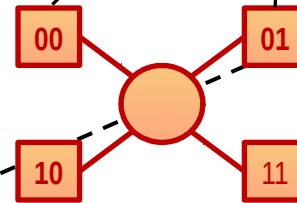
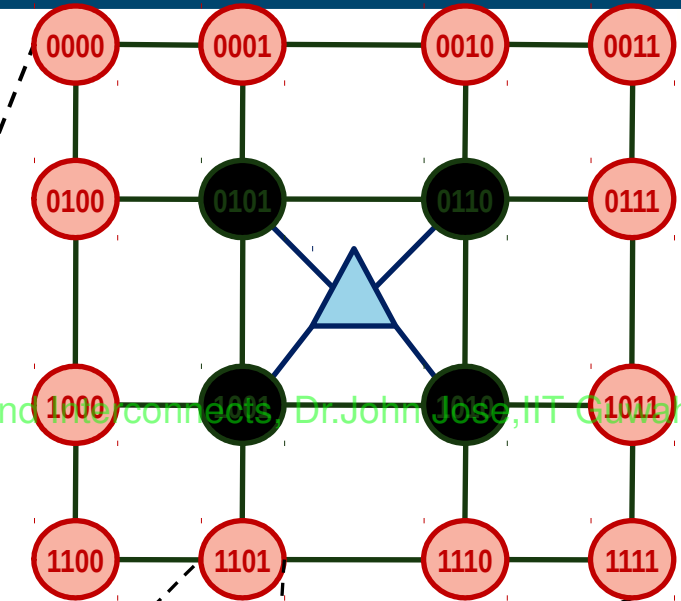
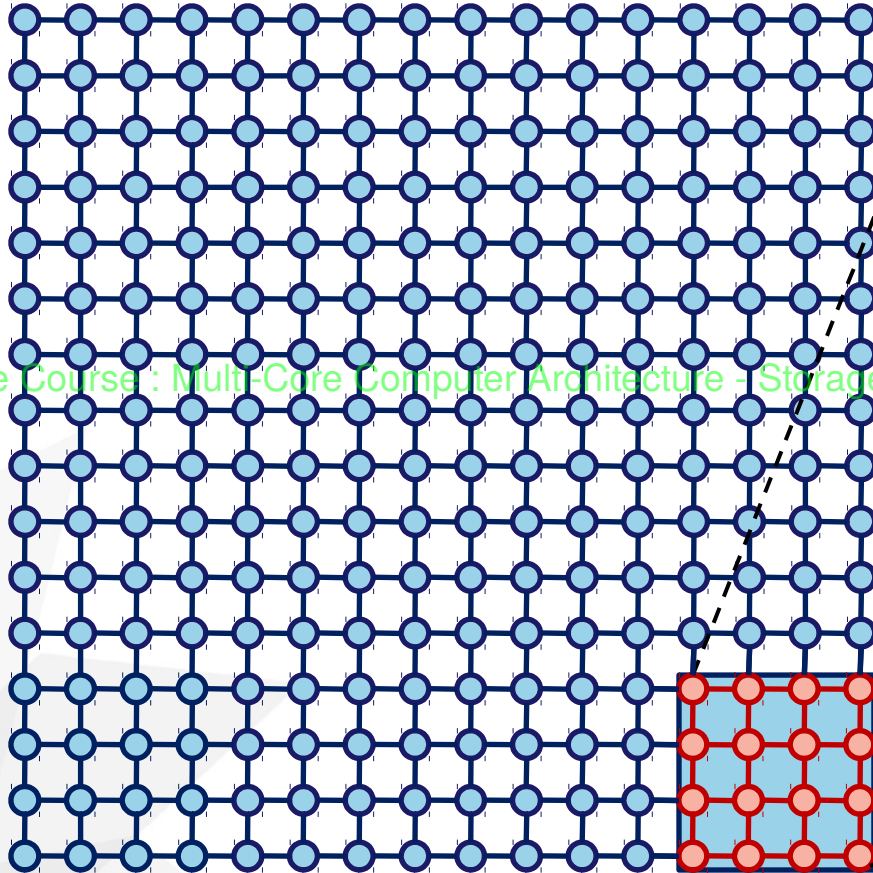


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16 X 16 Cmesh - 1024 cores

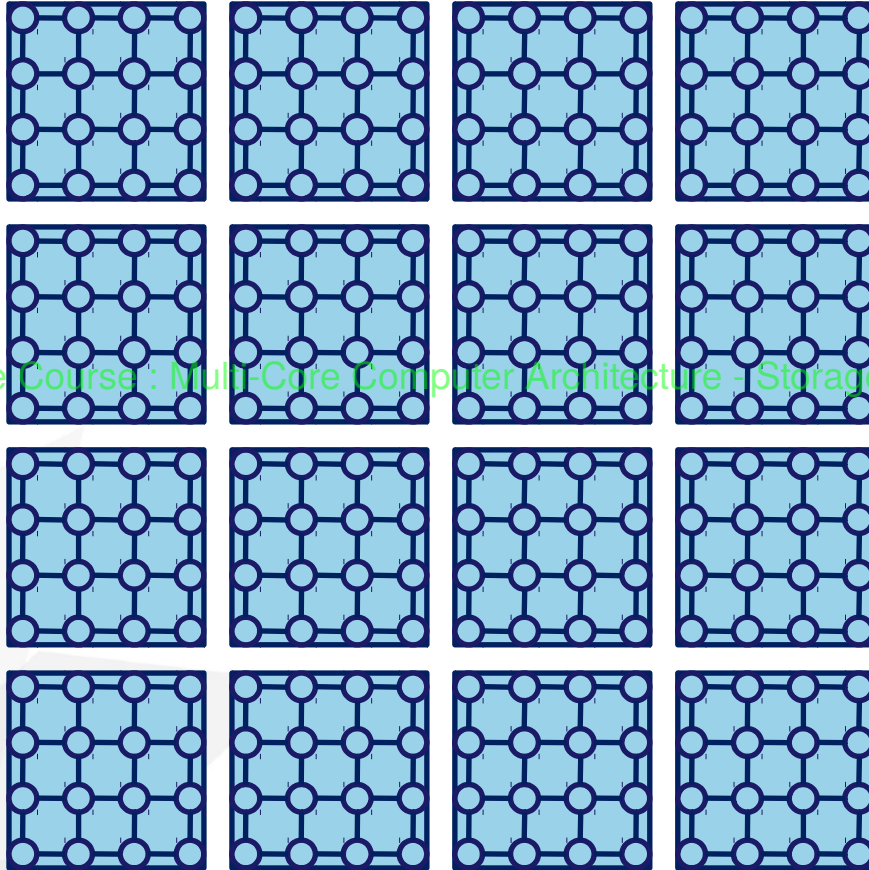


Wcube Structure



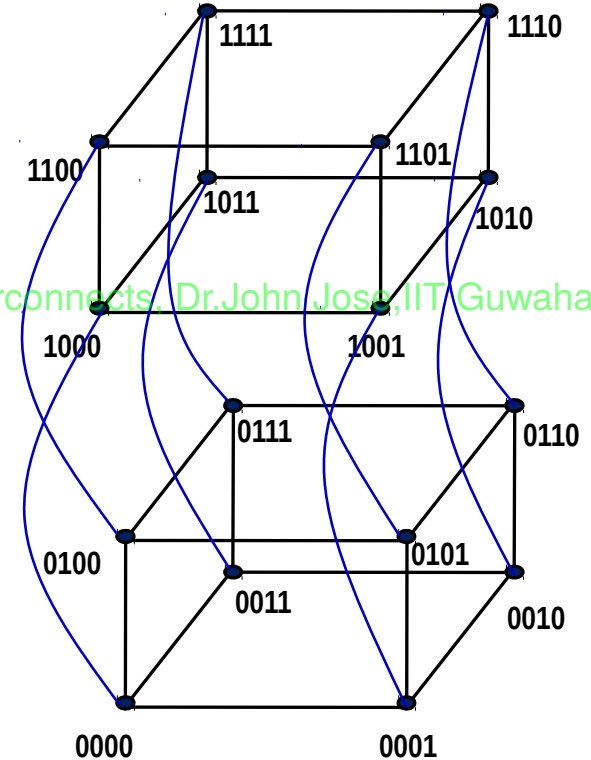
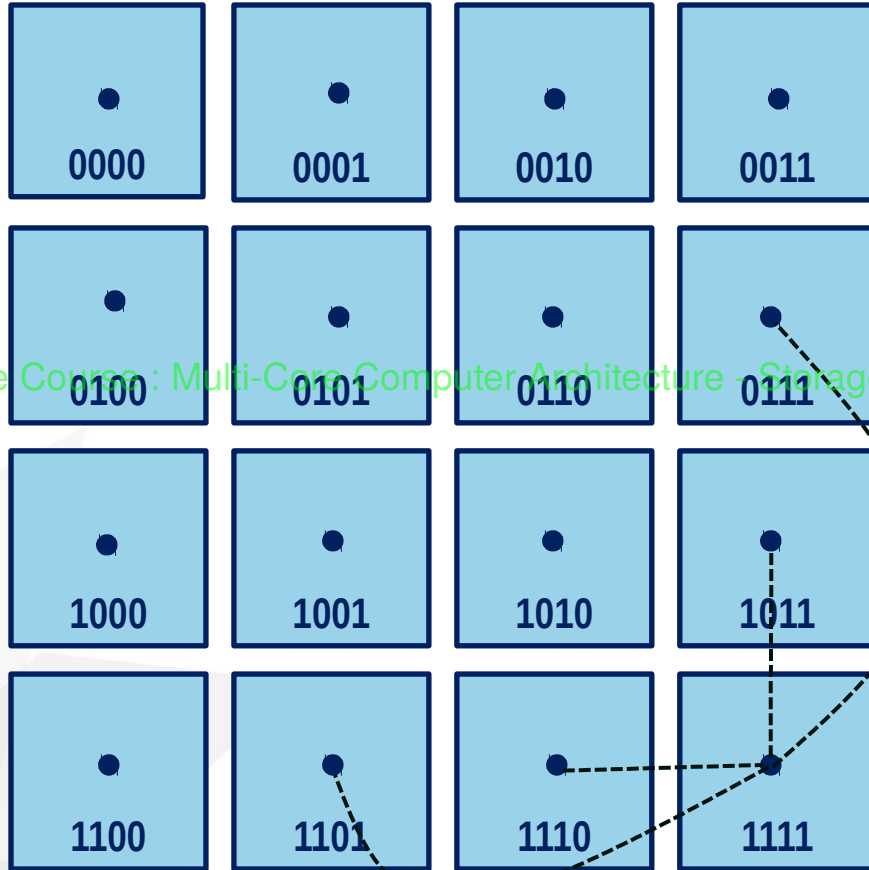
- -routers are connected to computing nodes
- -routers are connected to shared L2 nodes

Wcube Structure

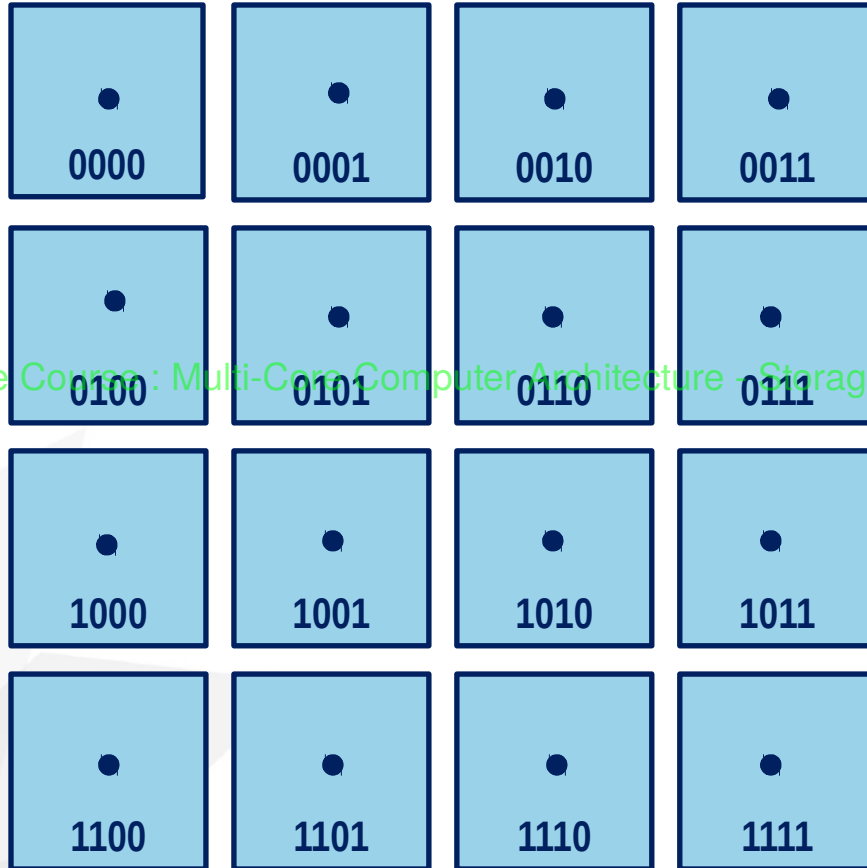


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Wcube Structure

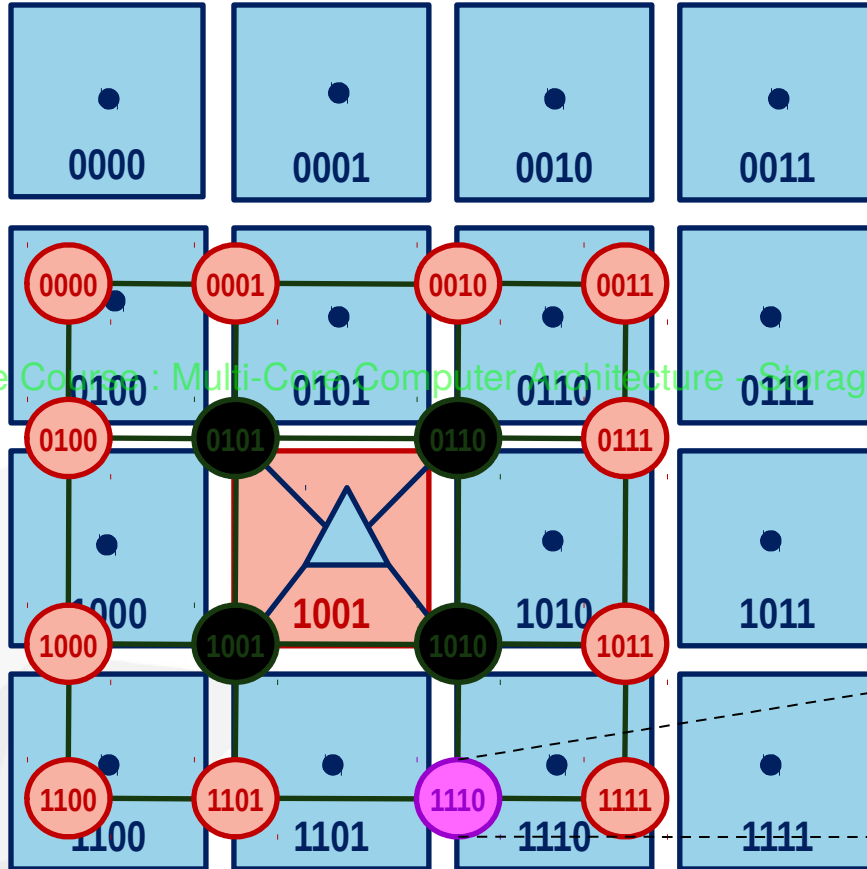


Wcube Structure

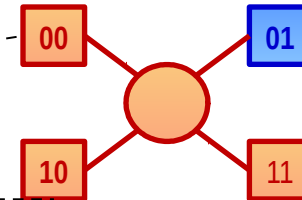


- Address of a node is presented as
1001.1110.01

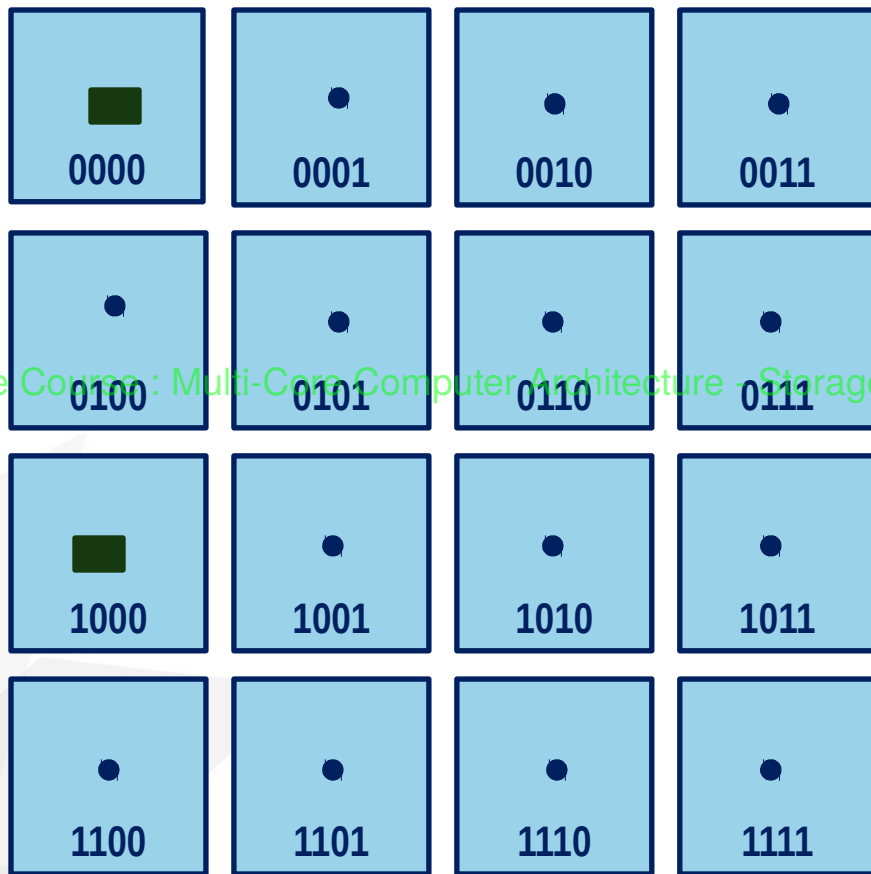
Wcube Structure



- Address of a node is presented as
1001.1110.01

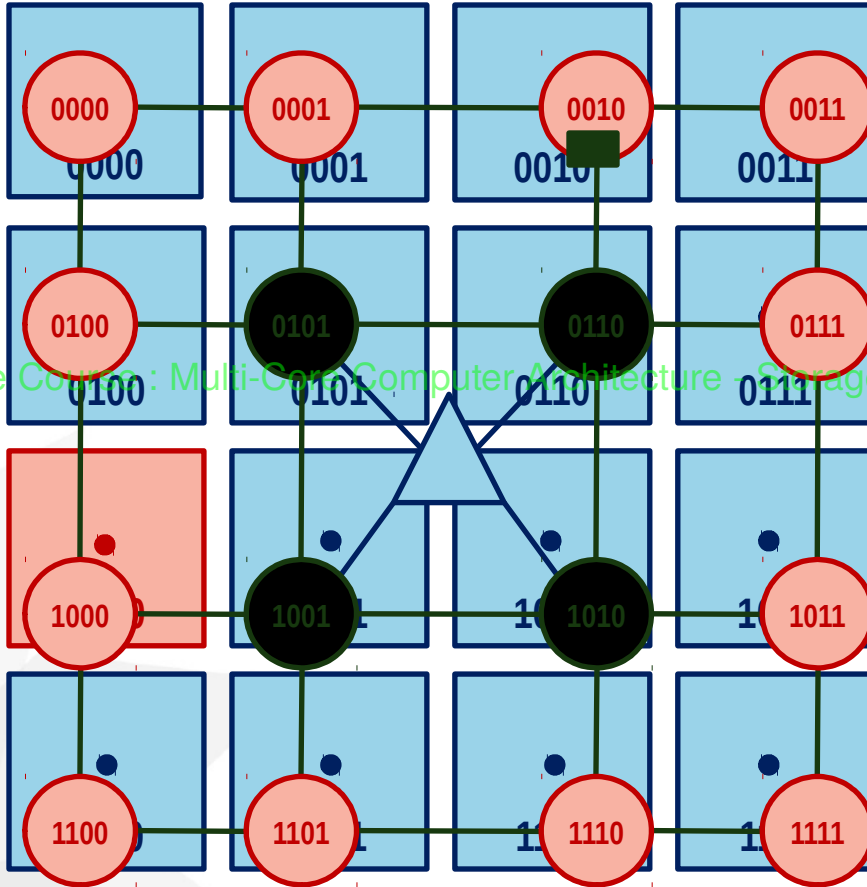


Deadlock free routing in each level



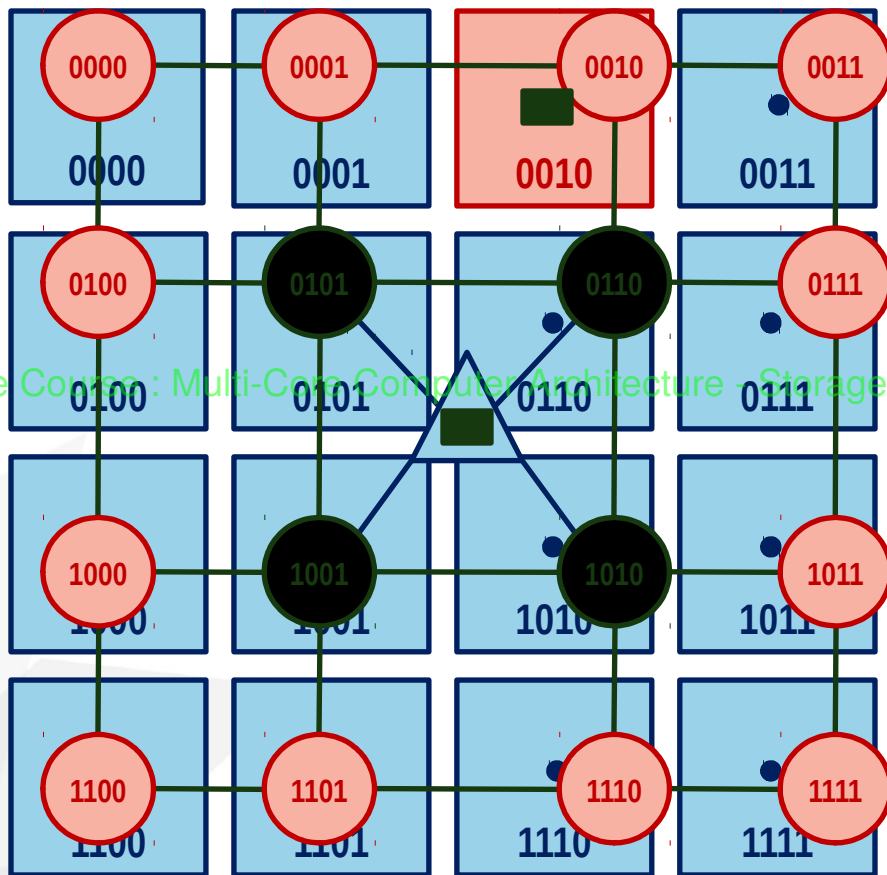
- If a packet wants to travel from **1000.0010.11** to **0010.0110.01**
- The packet reaches transmitter of Wcube-**1000** (in 2 hop)
- Then it follows path
1000 → **0000**
0000 → **0010** (in 2 hop)

Deadlock free routing in each level



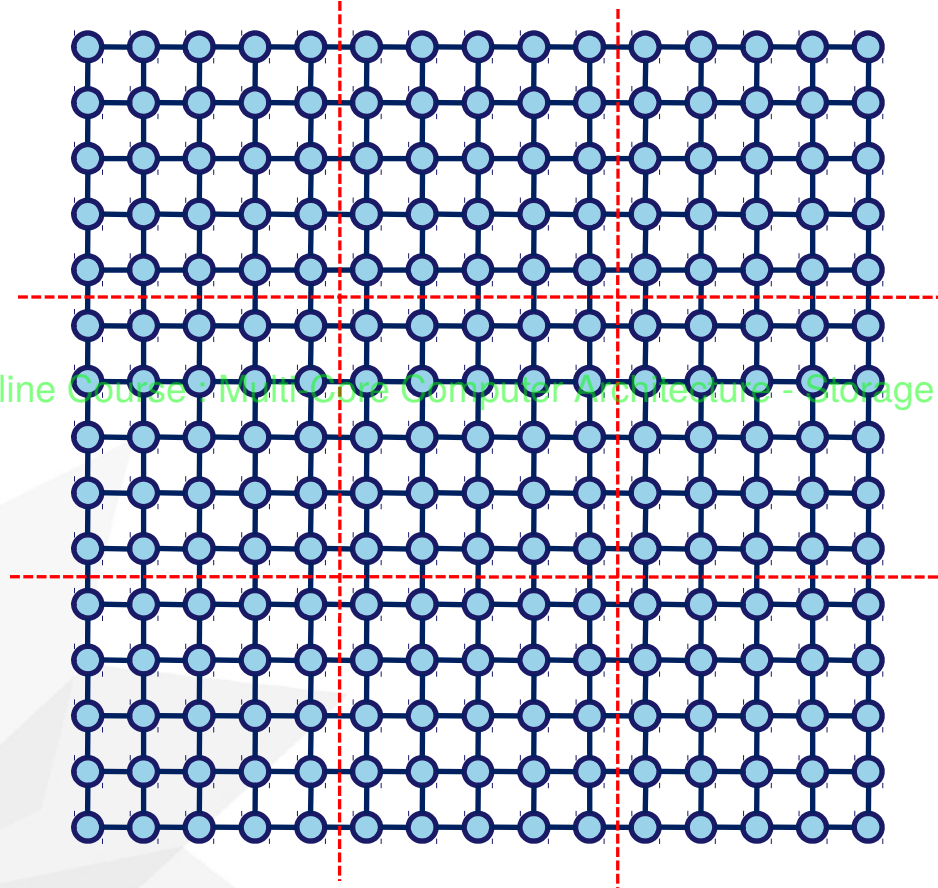
- If a packet wants to travel from **1000.0010.11** to **0010.0110.01**
- The packet reaches transmitter of Wcube-**1000** (in 2 hop)

Deadlock free routing in each level



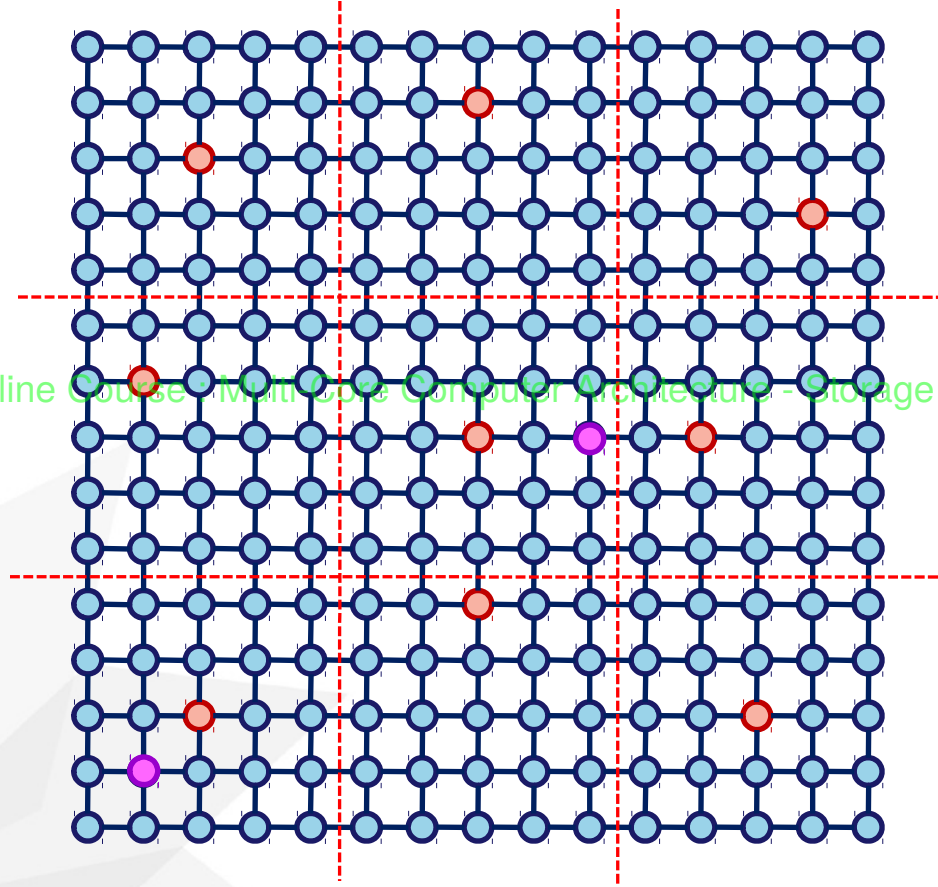
- If a packet wants to travel from **1000.0010.11** to **0010.0110.01**
- The packet reaches transmitter of Wcube-**1000** (in 2 hop)
- Then it follows path
1000 → **0000**
0000 → **0010** (in 2 hop)
- From the receiver of **0010** it reaches **0010.0110.01** (in single hop)
- Every cache miss request or reply packet reaches its destination in minimum **1** to maximum **8** hops

Small world architecture



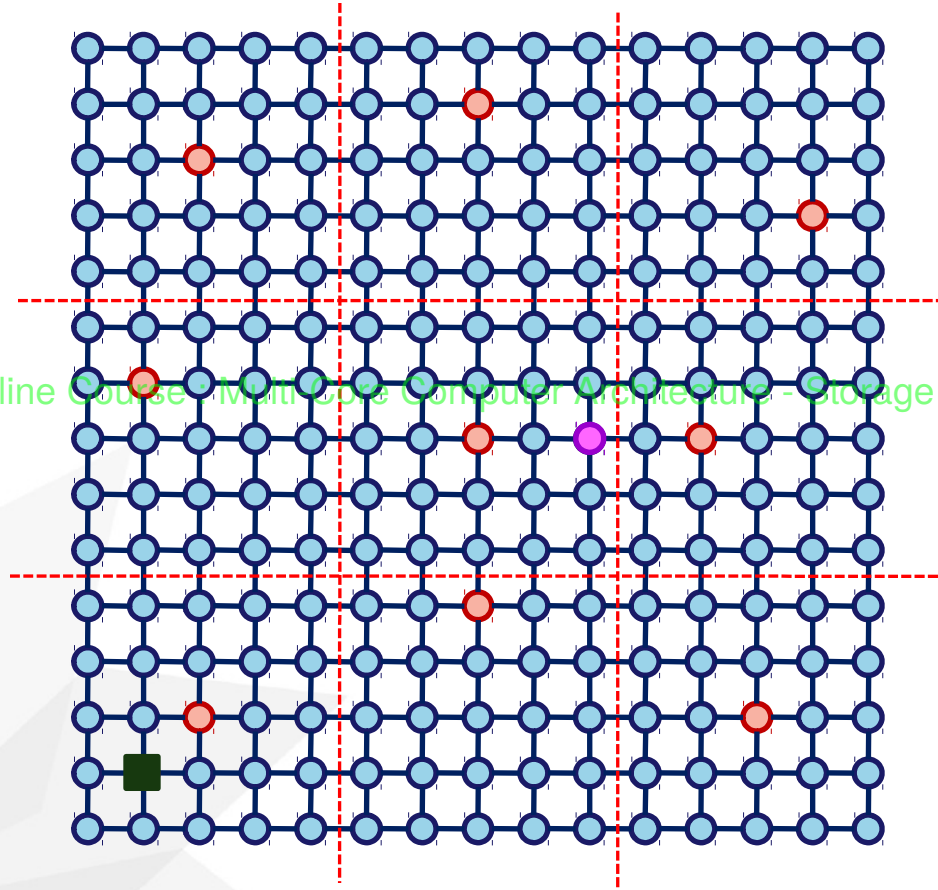
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Small world architecture



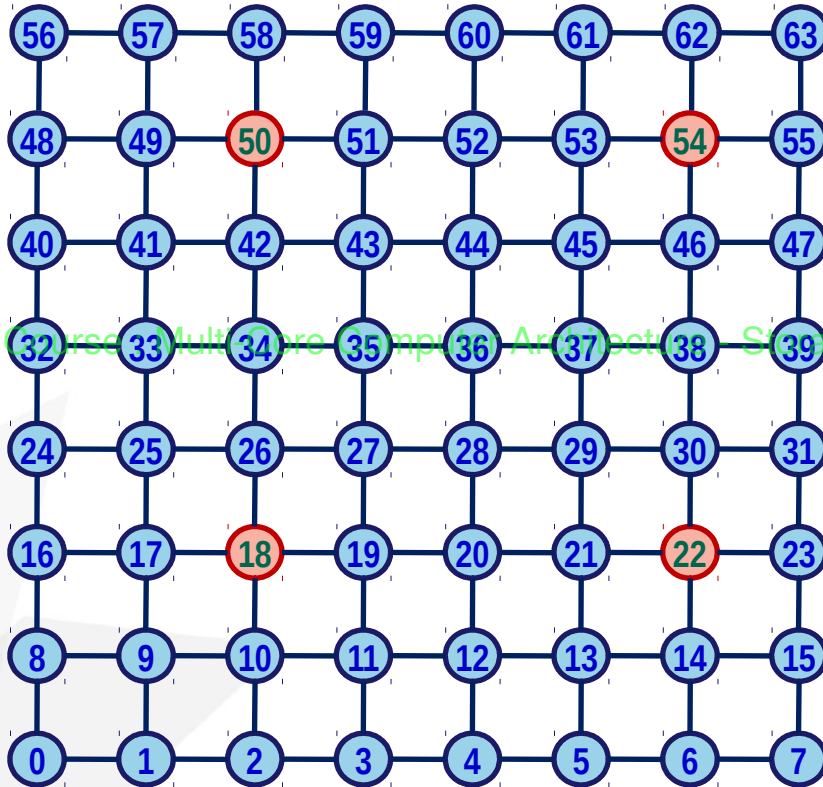
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Small world architecture



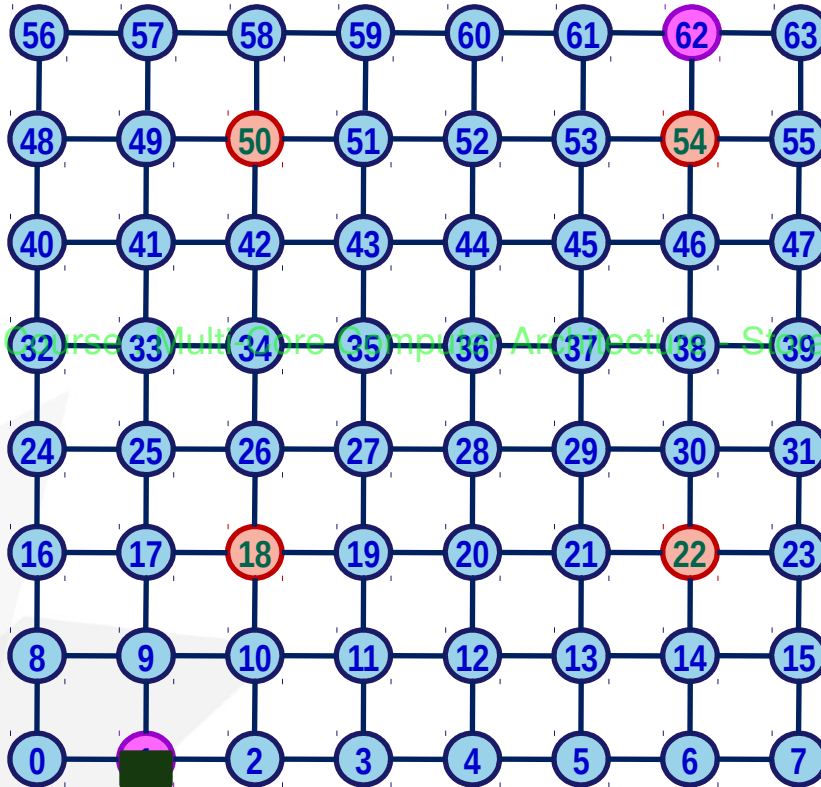
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8x8 mesh with Wireless Routers

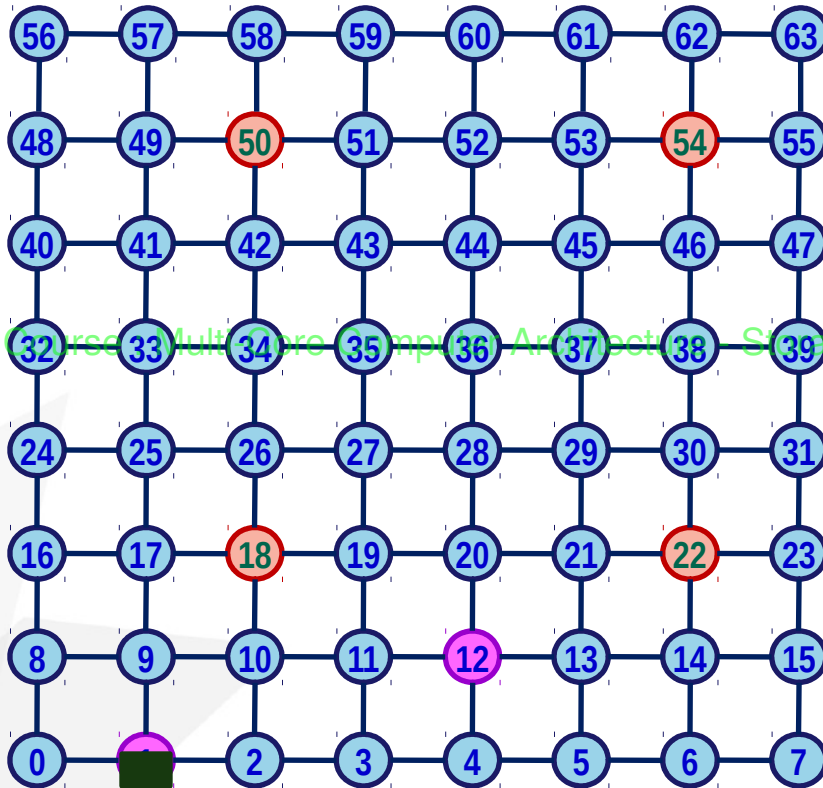


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8x8 mesh with Wireless Routers

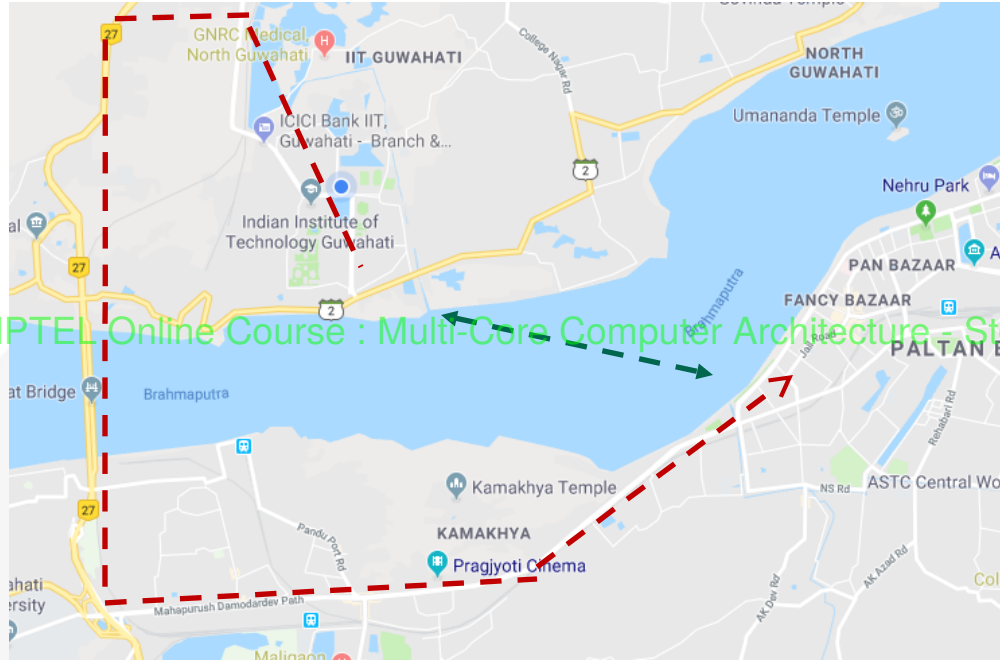


8x8 mesh with Wireless Routers



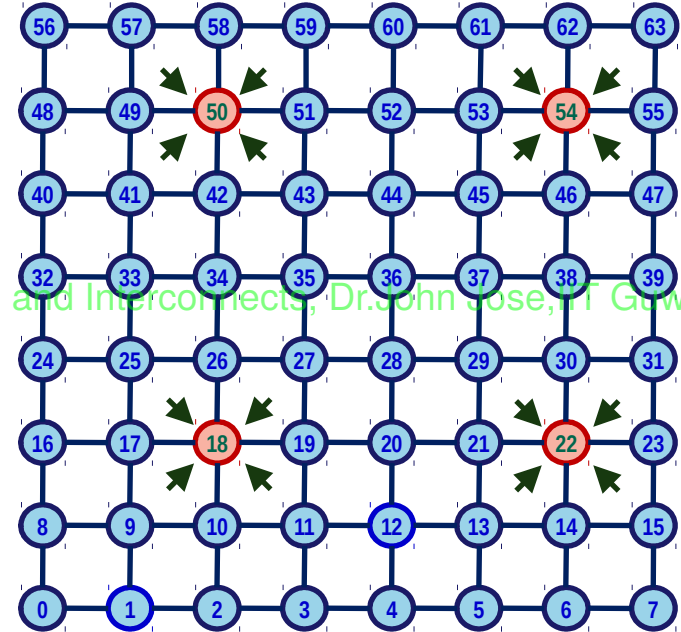
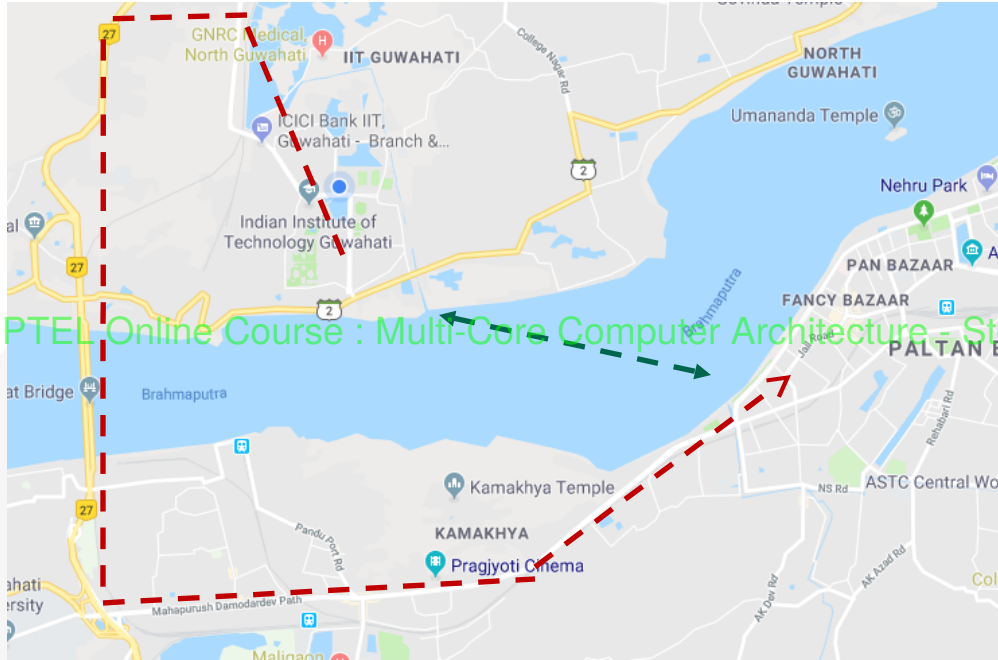
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A real life example



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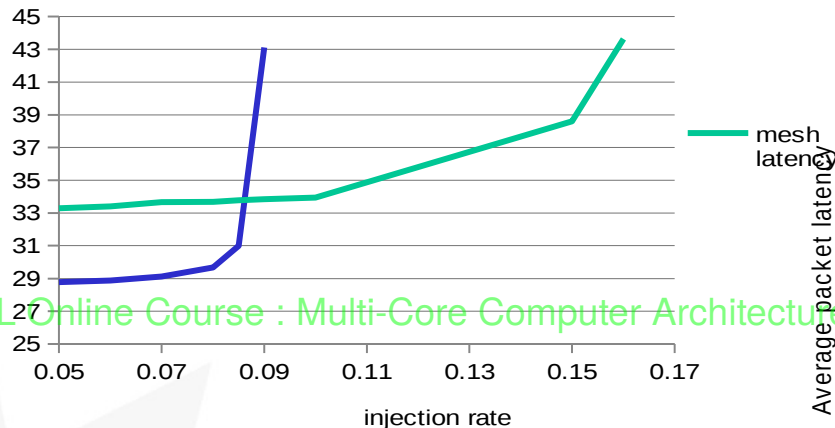
Isolated points of congestion



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Injection-rate vs. Latency

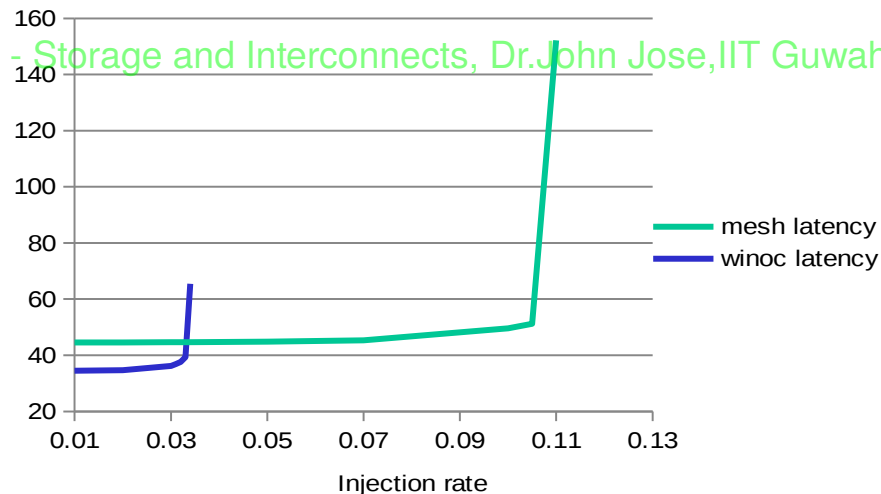
Average packet latency



64 cores uniform traffic (26%)

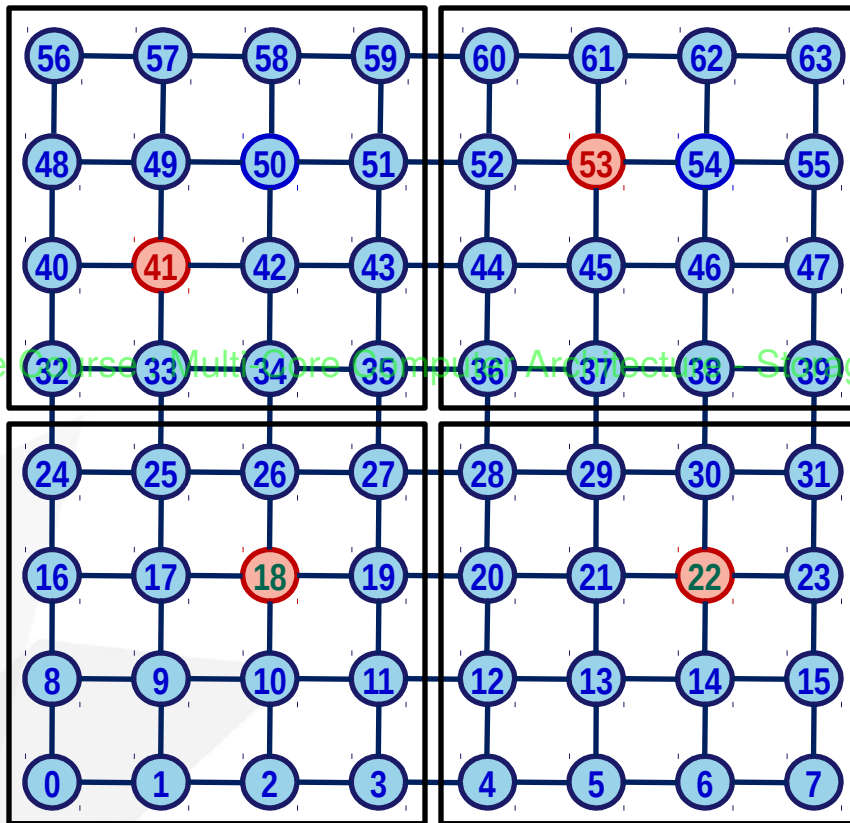
❖ How to minimize congestion in wireless links by dynamically selecting wireless path ?

Average packet latency

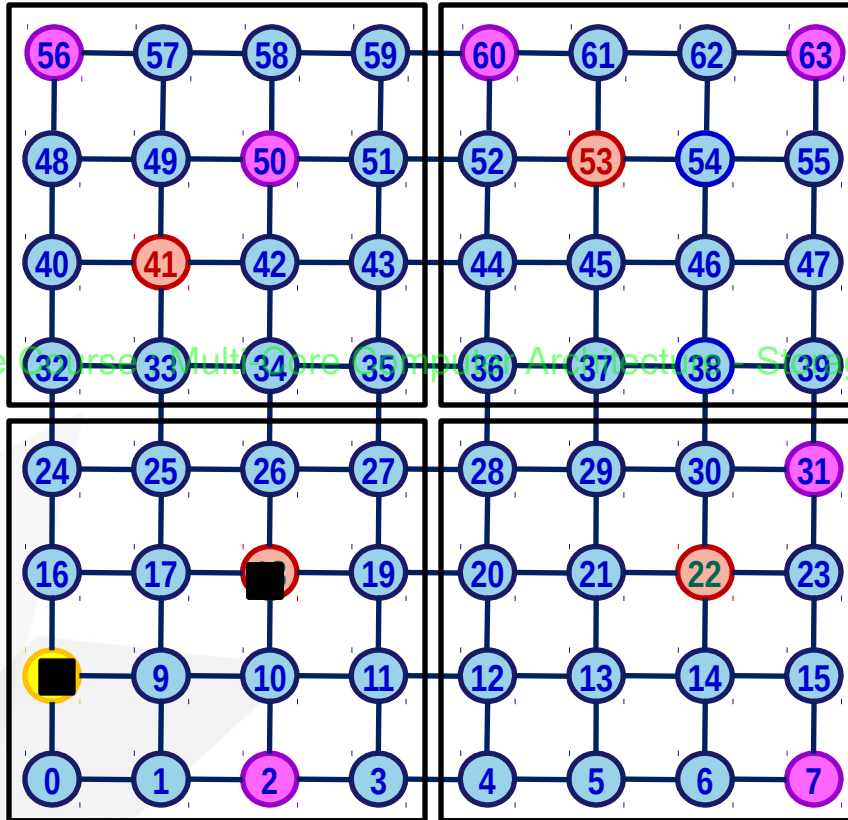


64 cores tornado traffic (54%)

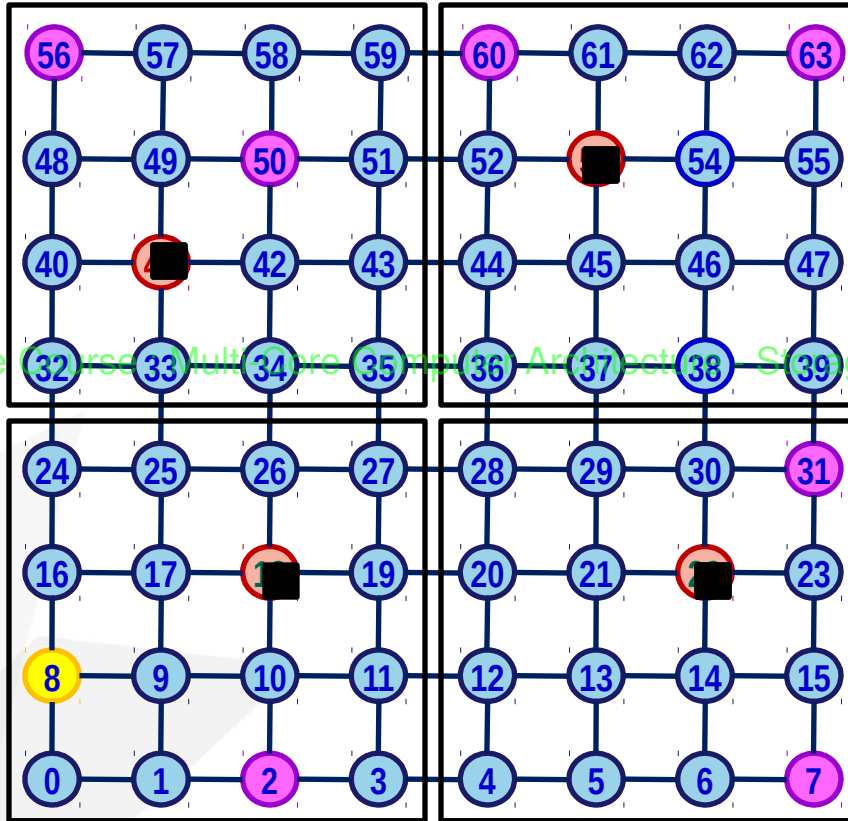
Multicasting using WiNoC



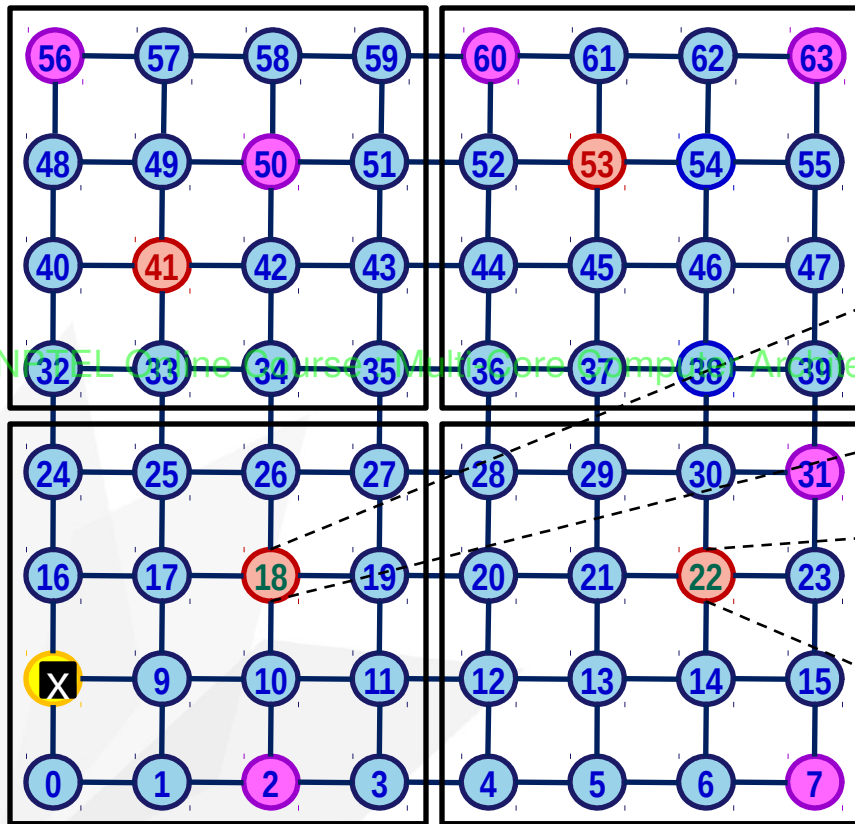
Multicasting using WiNoC



Multicasting using WiNoC



Multicasting in cache coherence

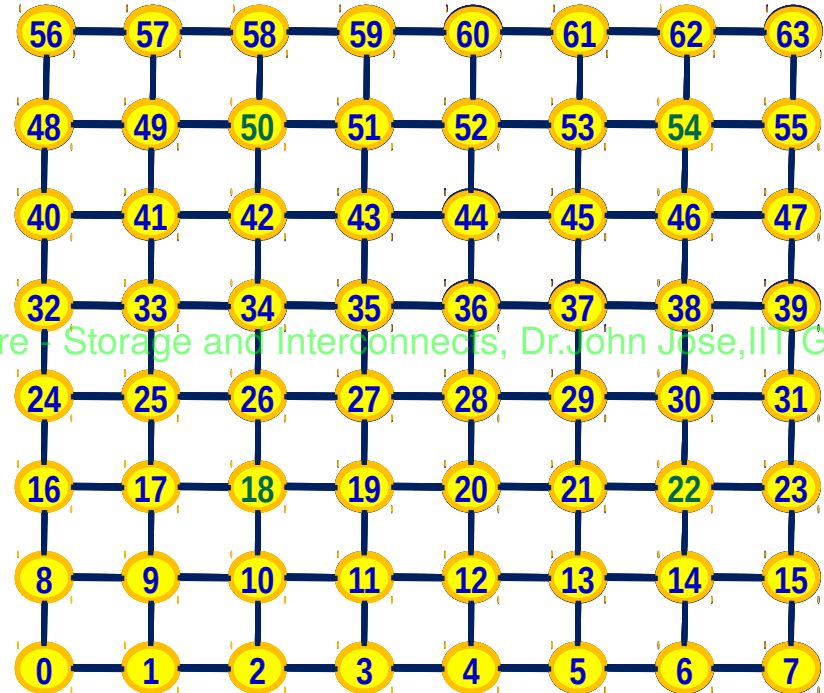
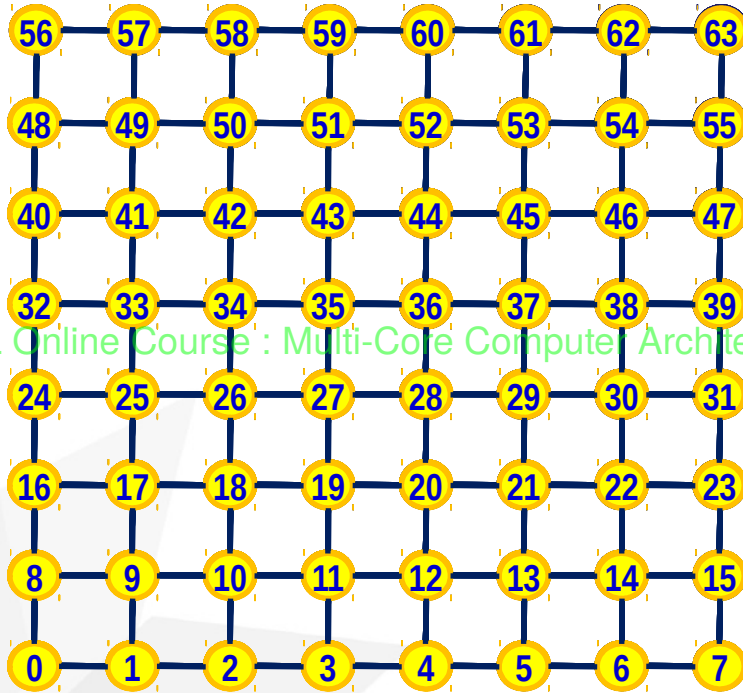


A	D	0	1	2	3	8	9	10	11	16	17	18	19	24	25	26	27
x	1	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0

A	D	4	5	6	7	12	13	14	15	20	21	22	23	28	29	30	31
x	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1

Shreedhar, T., & Deb, S. (2016). Hierarchical Cluster Based NoC Design Using Wireless Interconnects for Coherence Support. *Proceedings of the IEEE International Conference on VLSI Design, 2016–March*, 63–68

Broadcasting in a mesh vs WNoC



Summary

- ❖ Multicore processors and on chip clouds are going to become an integral part of future digital technologies.
- ❖ Understanding the hardware of such system will help us to
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design with conceptual clarity.
- ❖ Our country need good computer architects and processor design engineers with hands on exposure to VLSI design flow to cater the growing demand of skilled personnel in this domain.

How to explore computer architecture ?

- ❖ Refer to IEEE/ACM transactions & journals
 - ❖ IEEE TCAD, IEEE-TVLSI, IEEE-TOC, JPDC, JSC
 - ❖ ACM-TODAES, ACM-TECS, ACM-TACO
- ❖ Refer to top tier conferences
 - ❖ ISCA, HPCA, MICRO, ASPLOS, PACT, DATE, DAC, ICCAD
 - ❖ NOCS, NoCAD, ISVLSI, ICCD, ASPDAG, VLSI-SoC, GLSVLSI, HiPC, VLSID, VDAT, ISED
- ❖ Familiarize open source architectural simulators
 - ❖ GEM5, Multi2sim, Sniper, Tejas,
 - ❖ Booksim, DRAMSim, Usimm
 - ❖ Cacti, Orion
- ❖ Model the architecture in simulators and implement them using HDLs, Verify sub-modules in FPGA kit explore further ...

**THANK
YOU!**

FOR

**YOUR
PRESENCE**

johnjose@iitg.ac.in

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